Memory-Optimal Sequential Synthesis of Multimode Gaussian Transformations

Fucheng Guo [*] and Frank Mueller [†]
Department of Computer Science, North Carolina State University, Raleigh, North Carolina 27695, USA

Yuan Liu [‡]
Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695, USA
Department of Computer Science, North Carolina State University, Raleigh, North Carolina 27695, USA and
Department of Physics and Astronomy, North Carolina State University, Raleigh, North Carolina 27695, USA

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In modular quantum computing architectures, communication between hardware modules is mediated by traveling qumodes sent through transmission lines. Each output qumode interacts with the emitting module only once through a beam-splitter-type interaction and becomes inaccessible to that module after emission. Information required for subsequent outputs must therefore remain in long-lived memory qumodes. For a prescribed multimode Gaussian transformation on N qumodes, this work determines the minimum memory cost for any given emission order, constructs an explicit sequential protocol attaining this minimum, and develops a greedy method for identifying memory-efficient emission orders. The transformation is represented by a symplectic matrix S, specified either directly or through a Gaussian gate sequence. The exact minimum memory cost is obtained from the ranks of submatrices of S and further reduces to a support-based counting rule whose computational cost is linear in the size of the support data. When S is specified directly, a matrix-based protocol attains the minimum memory cost. If instead S is specified through a gate sequence, the original gates can be reused without additional synthesis, although the resulting memory usage need not be minimal. Gaussian transformations with local support on a D-dimensional cubic lattice can be realized sequentially with $O(N^{(D-1)/D})$ memory qumodes. The protocols also apply to non-Gaussian inputs, including GKP and cat states, and thereby provide an explicit, resource-efficient scheme for intermodule communication in modular architectures for universal continuous-variable quantum computation.

I. INTRODUCTION

Modular quantum architectures provide a scalable approach to building large quantum systems from smaller, independently controlled modules [1, 2]. Quantum states can be stored and processed within individual modules and transmitted between them as traveling qumodes through transmission lines [3–7]. In many applications, a module emits multiple traveling qumodes whose entanglement structure is established by a multimode Gaussian transformation [8–13]. Here, Gaussian refers to the operations used to establish entanglement among the qumodes, rather than to the states carried by the individual qumodes locally. The input qumodes may therefore carry arbitrary states, including non-Gaussian states such as Gottesman–Kitaev–Preskill (GKP) states [14–16] and cat states [6]. The resulting multimode state may likewise be non-Gaussian, even though the entanglement among qumodes is generated by Gaussian operations [6, 15, 16].

Consider a general multimode Gaussian transformation acting on N input qumodes. In phase space, the transformation is represented by a symplectic matrix $S \in \mathrm{Sp}(2N, \mathbb{R})$ that maps the input quadratures to those of the N output qumodes [17–19]. The transformation can be decomposed into phase-space rotations, single-qumode squeezing operations, and beam-splitter (BS) interactions [18, 20]. These operations can be implemented on stationary qumodes and controlled on demand [21, 22].

The output qumodes are emitted sequentially as traveling qumodes. Depending on the physical platform, stored states may be released through tunable coupling to a transmission line or through parametric mode conversion, while spontaneous and drive-assisted emission are commonly used to generate traveling qumodes directly [6, 23–26]. The present work considers a state-independent BS-type release, in which a BS interaction transfers the state of a stationary qumode to a traveling qumode through parametrically controlled mode conversion [6, 7]. After the transfer, the emitted qumode is no longer accessible to the emitting module. The stationary qumodes retained in the module and reused throughout the sequential implementation are referred to here as memory qumodes. For a given multimode Gaussian transformation, this loss of access raises three central questions: (1) How can an emission order requiring few memory qumodes be found? (2) For a chosen emission order, what is the minimum number of memory qumodes required? (3) How can a sequential protocol achieving this minimum be constructed?

Previous studies of sequential generation have mainly

* fguo22@ncsu.edu
† fmuelle@ncsu.edu
‡ q_yuanliu@ncsu.edu

focused on preparing a prescribed target state [27, 28]. Matrix-product-state (MPS) methods describe such processes in terms of the dimension of an auxiliary system, with analogous formulations available for Gaussian states [27–29]. Related work has also studied the minimum number of emitters required to generate photonic graph states [30, 31]. Large-scale optical experiments have further demonstrated the sequential generation of specific one- and two-dimensional continuous-variable cluster states [10–13], establishing the scalability of this approach for particular families of target states.

The problem considered here is different. MPS-based methods may characterize the sequential generation of an individual output state [27–29], but they do not by themselves characterize the sequential implementation of a prescribed multimode Gaussian transformation for arbitrary input states. In the present setting, the relevant resource is the number of reusable memory qumodes required to preserve the information needed for outputs that have not yet been emitted. Existing state-preparation results therefore do not determine the minimum memory cost of implementing a general symplectic transformation, account for its dependence on the emission order, identify an emission order with low memory cost, or construct a sequential protocol guaranteed to attain the minimum [10–13, 27–31].

This work contributes an analysis that establishes how to determine the minimum memory cost for any prescribed emission order and constructs a sequential protocol that attains this minimum. It also develops an efficient method for identifying emission orders with low memory cost. These results are demonstrated through two applications: continuous-variable quantum error-correcting encoders, which map logical information into multimode code spaces that enable error detection and correction [15, 16, 32, 33], and the sequential generation of continuous-variable cluster states, which provide a key resource for measurement-based quantum computation [8, 9].

The main results of this work are as follows. First, for any $S \in \mathrm{Sp}(2N,\mathbb{R})$ and any prescribed emission order, the minimum number of memory qumodes is given by one-half of the maximum rank of a corresponding family of submatrices of S (Sec. III). This rank expression further reduces to a simple counting rule based on the support pattern of S. Consequently, the minimum memory cost can be evaluated in time linear in the size of the support data, without explicit rank calculations. Second, two sequential synthesis protocols are developed. The gate-sequence protocol presented in Sec. IV reuses the gates of a given Gaussian circuit without additional synthesis, although its memory usage need not be minimal. The matrix-based protocol in Appendix A constructs new in-register Gaussian operations from the target symplectic matrix and always achieves the minimum memory cost. Third, the memory cost depends strongly on the emission order. A deterministic greedy heuristic is developed to identify memory-efficient emission orders (Secs. V and VI). Finally, Gaussian transformations with local support on a D-dimensional cubic lattice can be realized sequentially with $O(N^{(D-1)/D})$ memory qumodes (Sec. VII).

II. MODEL AND SETUP

A. Gaussian Transformation and Sequential Architecture

A Gaussian unitary acting on N bosonic qumodes is represented in phase space by a symplectic matrix $S \in \mathrm{Sp}(2N,\mathbb{R})$ [9, 15]. Defining the quadrature vector

$$\hat{\mathbf{r}} = (\hat{q}_1, \hat{p}_1, \ldots, \hat{q}_N, \hat{p}_N)^\top, \tag{1}$$

with $[\hat{q}_j, \hat{p}_k] = i\,\delta_{jk}$ and $[\hat{q}_j, \hat{q}_k] = [\hat{p}_j, \hat{p}_k] = 0$, the transformation is

$$\hat{\mathbf{r}} \mapsto S\,\hat{\mathbf{r}}, \qquad S^\top \Omega S = \Omega, \qquad \Omega = \bigoplus_{j=1}^{N} \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix}. \tag{2}$$

The target Gaussian transformation is specified by S. The input states are determined by the chosen code and are not included in S.

To implement S, the N output qumodes are generated sequentially [34]. They are produced using a small set of stationary, reusable memory qumodes on which arbitrary Gaussian operations can be performed [21, 35]. Each output is transferred to a separate traveling qumode that is initially in the vacuum state and interacts once, through a full swap, with the memory qumode carrying that output before leaving the module. As shown schematically in Fig. 1, the initial input qumodes are first loaded into the memory register. At each step, Gaussian operations within the register map the next output o_k onto one memory qumode while retaining the information required for later outputs in the remaining memory qumodes. A beam-splitter full swap then transfers o_k to the vacuum traveling qumode and leaves the corresponding memory qumode in the vacuum state. When additional inputs are required, new input qumodes can be injected into available memory qumodes before the next register operation. The number and timing of these injections may vary from step to step according to the target transformation and emission order.

B. Emission of Traveling Qumodes

The release is implemented by a BS interaction. As a concrete realization, in circuit quantum electrodynamics (QED) [5–7], driving the Josephson nonlinearity at the frequency difference between a memory qumode a and a traveling qumode b gives the rotating-frame Hamiltonian

$$H(t)/\hbar = g(t)\,\hat{a}^\dagger \hat{b} + g^*(t)\,\hat{a}\,\hat{b}^\dagger, \tag{3}$$

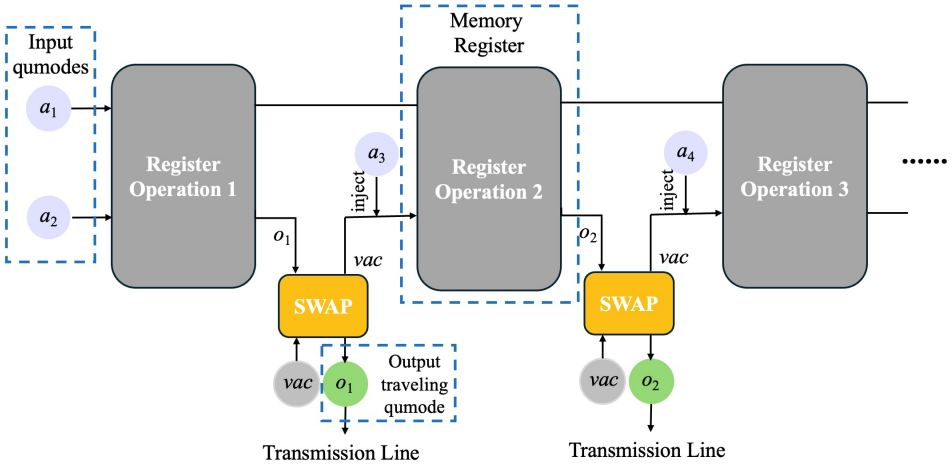

FIG. 1. Sequential implementation of a multimode Gaussian transformation S using a reusable memory register. The memory register consists of stationary qumodes on which Gaussian operations can be performed. Time proceeds from left to right. The initial input qumodes are first loaded into the register. At each step, an in-register Gaussian operation maps the next output qumode o_k onto one memory qumode while retaining the information required for later outputs in the remaining memory qumodes. The state of o_k is then transferred to a vacuum traveling qumode through a beam-splitter full swap ($\theta = \pi$, labeled "SWAP") and released into a transmission line. The swap leaves the corresponding memory qumode in the vacuum state, which can then be replaced by a newly injected input qumode and reused in the next register operation. Repeating this procedure emits the outputs sequentially in the prescribed order $o_1, \ldots, o_N$. After emission, each traveling qumode is no longer accessible to the emitting module.

where $\hat{a}$ and $\hat{b}$ are the corresponding annihilation operators. The complex coupling amplitude $g(t)$ is controlled by the strength and phase of the parametric pump and can be switched on and off on demand [6, 21, 22]. Since the phase of $g(t)$ can be absorbed into the definition of the traveling qumode, the corresponding beam-splitter gate may be written as

$$\begin{aligned} \hat{U}_{\mathrm{BS}}(\theta) &= \exp\left[-i\frac{\theta}{2}\left(\hat{a}^\dagger\hat{b} + \hat{a}\hat{b}^\dagger\right)\right], \\ \theta &= 2\int_0^\tau |g(t)|\,\mathrm{d}t, \end{aligned} \tag{4}$$

where τ is the duration of the beam-splitter pulse.

In this work, each emission is required to transfer the state of the memory qumode completely to the traveling qumode and leave the memory qumode in the incoming vacuum state. This is achieved by choosing $\theta = \pi$, for which the beam-splitter gate implements a full swap. Because Eq. (3) is bilinear in the annihilation operators, the swap implements a fixed symplectic transformation that is independent of the state being released [6]. Thus, each traveling qumode interacts with the memory register exactly once and, after emission into the transmission line, can no longer be operated on by the emitting module.

C. Memory Cost for a Fixed Emission Order

Because emitted qumodes cannot be accessed again, the emission order affects the required memory. Let $S[o, a]$ denote the 2×2 block of S that maps input qumode a to output qumode o. The support of output o is defined as

$$\mathrm{supp}(o) = \{\, a : S[o, a] \neq 0 \,\}. \tag{5}$$

For the exact implementation considered here, the support is determined solely by whether or not a block is zero as every nonzero block $S[o, a]$ is included in $\mathrm{supp}(o)$, regardless of its magnitude. As a result, even very small nonzero blocks can enlarge the support and increase the predicted memory cost. When many such blocks are present, an approximate implementation may therefore provide a more practical description. One possible approach is to choose a matrix norm and a threshold $\varepsilon > 0$, and define

$$\mathrm{supp}_\varepsilon(o) = \{a : \|S[o, a]\| > \varepsilon\}, \tag{6}$$

so that blocks satisfying $\|S[o, a]\| \leq \varepsilon$ are neglected. This thresholded support may reduce the required memory, but it also perturbs the target transformation. A complete treatment would therefore require quantifying the resulting implementation error, determining how it accumulates across the protocol, and analyzing its dependence on the input state. Such an approximate formulation is beyond the scope of the present work, which focuses on exact implementations.

To implement S faithfully, every input in $\mathrm{supp}(o)$ must be present in the register before o is emitted. Thus, when the k-th output o_k is released, the set of injected inputs is

$$P_k = \bigcup_{j \leq k} \mathrm{supp}(o_j), \tag{7}$$

while the outputs that remain to be emitted are $F_k = \{o_k, \ldots, o_N\}$.

Although inputs could be injected earlier, doing so cannot reduce the required memory. A memory-optimal protocol therefore injects each input only when it is first needed, so Eq. (7) gives the injected set at every step. The correlations that must remain in the register at the k-th emission are described by the submatrix $S[F_k; P_k]$, whose rows correspond to the quadratures of the outputs in F_k and whose columns correspond to those of the inputs in P_k. Since these inputs cannot be injected again and these outputs have not yet been released, the memory register is the only system that can retain these correlations. The rank of $S[F_k; P_k]$ counts the number of independent quadratures involved, and the factor of $\frac{1}{2}$ converts these quadratures into conjugate pairs, one pair per memory qumode. Thus, $\frac{1}{2}\operatorname{rank} S[F_k; P_k]$ is the natural candidate for the number of memory qumodes required at this step. The next section proves that this rank is even and that this candidate is exact. The largest value of this quantity over the emission sequence is therefore the natural candidate for the memory cost of implementing S in the chosen order.

Section III shows that this candidate is exact: No faithful implementation can use fewer memory qumodes, and an explicit protocol achieves the bound. The same section also reduces the rank expression to a simple count, namely the number of inputs injected so far minus the number of outputs already emitted.

III. MINIMUM NUMBER OF MEMORY QUMODES

Section II showed that, before the k-th output is emitted, the memory register must preserve the correlations described by the submatrix $S[F_k; P_k]$. These correlations require at least $\frac{1}{2}\operatorname{rank} S[F_k; P_k]$ memory qumodes at that step. Therefore, the largest of these quantities over the full emission sequence is a lower bound on the memory cost for the chosen emission order. It is not immediate that this lower bound can actually be achieved, because the memory must preserve the correct information not only for the current output but also for all later outputs. The following theorem proves that a single sequential protocol can always achieve this bound. A subsequent corollary reduces the rank expression to a simple count determined only by the support pattern of S.

Theorem 1 (Minimum number of memory qumodes)**.** *For a given emission order $o_1, \ldots, o_N$, the minimum number of memory qumodes required to realize $S \in \mathrm{Sp}(2N, \mathbb{R})$ faithfully under sequential emission by single full swaps is*

$$n_{\mathrm{mem}}(S) = \max_{1 \le k \le N} \frac{1}{2} \operatorname{rank} S[F_k; P_k], \tag{8}$$

where $P_k = \bigcup_{j \le k} \mathrm{supp}(o_j)$ and $F_k = \{o_k, \ldots, o_N\}$. Each rank $S[F_k; P_k]$ *is even, and therefore $n_{\mathrm{mem}}(S)$ is an integer.*

The proof consists of two parts. The lower bound shows that any faithful sequential implementation must use at least the number of memory qumodes in Eq. (8). The upper bound gives an explicit construction that achieves this value.

A. Lower Bound

At each emission step, any correlations between the inputs already injected and the outputs not yet emitted must be preserved in the memory register, which gives the lower bound on the required memory. To derive the lower bound, we describe the input and output quadratures in a common space, $V = \mathbb{R}^{2N}_{\mathrm{in}} \oplus \mathbb{R}^{2N}_{\mathrm{out}}$, where the two components correspond to the input and output phase spaces. We equip V with the symplectic form $\Omega_V = \Omega_{\mathrm{in}} \oplus (-\Omega_{\mathrm{out}})$. The transformation S is represented by its graph,

$$L = \{(\mathbf{r}, S\mathbf{r}) : \mathbf{r} \in \mathbb{R}^{2N}\}, \qquad \dim L = 2N. \tag{9}$$

The minus sign in Ω_V makes L a Lagrangian subspace. Indeed, for any $(\mathbf{r}, S\mathbf{r}), (\mathbf{r}', S\mathbf{r}') \in L$, $\mathbf{r}^\top \Omega \mathbf{r}' - (S\mathbf{r})^\top \Omega (S\mathbf{r}') = 0$ because $S^\top \Omega S = \Omega$, and $\dim L = \frac{1}{2}\dim V$. This representation is the Gaussian analogue of the Choi construction and allows the input–output correlations to be analyzed across the emission sequence [27–29, 36].

Consider the cut immediately before the k-th emission. The future subspace contains the remaining inputs $\bar{P}_k$ and the outputs $F_k = \{o_k, \ldots, o_N\}$ that have not yet been emitted. The past subspace W contains the injected inputs P_k and the previously emitted outputs $\bar{F}_k = \{o_1, \ldots, o_{k-1}\}$, the complement of F_k. Because each input is injected before its first use, $S[\bar{F}_k; \bar{P}_k] = 0$ by Eqs. (5) and (7).

The number of qumodes shared across this cut is

$$b_k = \tfrac{1}{2}\big[\dim \pi_W(L) - \dim(L \cap W)\big], \tag{10}$$

where $\pi_W(L)$ is the projection of L onto the past subspace, while $L \cap W$ is the part of L contained entirely in the past. Their dimension difference counts the past quadrature degrees of freedom that remain connected to the future; the factor $1/2$ converts quadrature pairs into qumodes. This is the Gaussian analogue of the bond dimension in a matrix-product-state description [27, 29].

Ordering the inputs as $(P_k, \bar{P}_k)$ and the outputs as $(\bar{F}_k, F_k)$ gives

$$S = \begin{pmatrix} S[\bar{F}_k; P_k] & 0 \\ S[F_k; P_k] & S[F_k; \bar{P}_k] \end{pmatrix}. \tag{11}$$

For $(\mathbf{r}, S\mathbf{r}) \in L$, the past component is $\big(\mathbf{r}_{P_k}, S[\bar{F}_k; P_k]\mathbf{r}_{P_k}\big)$. Since $\mathbf{r}_{P_k} \in \mathbb{R}^{2|P_k|}$ is arbitrary,

$\dim \pi_W(L) = 2|P_k|$. Here $|\cdot|$ denotes the number of elements of a set.

A point of L lies entirely in W when $\mathbf{r}_{\bar{P}_k} = 0$ and $S[F_k; P_k]\mathbf{r}_{P_k} = 0$. Hence, $\dim(L \cap W) = 2|P_k| - \operatorname{rank} S[F_k; P_k]$. Substituting these dimensions into Eq. (10) gives

$$b_k = \tfrac{1}{2} \operatorname{rank} S[F_k; P_k]. \tag{12}$$

The symplectic Schmidt decomposition groups the shared quadratures into conjugate pairs [29, 37], so the rank is even and b_k is an integer.

At this cut, the memory register is the only system connecting the injected inputs P_k to the outputs F_k that remain to be emitted. A faithful implementation must therefore retain at least b_k memory qumodes. Maximizing over the sequence yields

$$n_{\mathrm{mem}}(S) \geq \max_k b_k = \max_k \tfrac{1}{2} \operatorname{rank} S[F_k; P_k]. \tag{13}$$

B. Upper Bound

A sequential construction is given that realizes S using at most $\max_k \frac{1}{2} \operatorname{rank} S[F_k; P_k]$ memory qumodes, thereby matching the lower bound derived above.

The rows of S form a symplectic frame. Since $S\Omega S^\top = \Omega$,

$$\{o_i, o_j\}_\Omega = \delta_{ij} \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix}. \tag{14}$$

Thus, the two quadratures of each output qumode satisfy the canonical commutation relation, while quadratures belonging to different output qumodes commute.

Consider the k-th emission step. The inputs in P_k have already been injected, and the outputs $o_1, \ldots, o_{k-1}$ have already been emitted. Since $\operatorname{supp}(o_k) \subseteq P_k$, the output o_k depends only on inputs already loaded into the device. It also commutes with every previously emitted output by Eq. (14). The injected input space can be decomposed into the emitted output qumodes and the qumodes still held in the register. Because o_k has no component along the emitted qumodes, it lies in the span of the current register qumodes.

A Gaussian operation within the register can therefore map o_k onto a single memory qumode without introducing an additional qumode. A π beam-splitter full swap then transfers this state to a vacuum traveling qumode, which is released as o_k. Equation (14) also implies that o_k commutes with all later outputs, so removing it does not disturb the information required for the remaining emissions. Repeating this procedure produces all outputs of S in the prescribed order.

It remains to bound the register size. Immediately before the k-th emission, $|P_k|$ inputs have been injected and $k-1$ outputs have been emitted, so the register contains $|P_k| - (k-1)$ memory qumodes. The restriction of S to the columns indexed by P_k has full column rank $2|P_k|$, since these columns are a subset of the linearly independent columns of S. The $2(k-1)$ rows associated with the emitted outputs are supported entirely on P_k and remain linearly independent. The remaining rows are those of $S[F_k; P_k]$, and therefore $\operatorname{rank} S[F_k; P_k] \geq 2|P_k| - 2(k-1)$. Hence, $|P_k| - (k-1) \leq \frac{1}{2} \operatorname{rank} S[F_k; P_k]$.

Taking the maximum over the emission sequence gives

$$n_{\mathrm{mem}}(S) \leq \max_k \tfrac{1}{2} \operatorname{rank} S[F_k; P_k]. \tag{15}$$

Together with the lower bound in Eq. (13), this proves Eq. (8). Appendix A gives the construction as an explicit algorithm.

C. Counting Form

The rank expression in Eq. (8) can be evaluated without performing any rank computation.

Corollary 1 (Counting form of the minimum)**.** *For every $S \in \mathrm{Sp}(2N, \mathbb{R})$, every emission order, and every step k,*

$$\tfrac{1}{2} \operatorname{rank} S[F_k; P_k] = |P_k| - (k-1).$$

Therefore,

$$n_{\mathrm{mem}}(S) = \max_{1 \leq k \leq N} \big(|P_k| - k + 1\big). \tag{16}$$

Proof. The upper-bound argument established $\operatorname{rank} S[F_k; P_k] \geq 2|P_k| - 2(k-1)$.

For the opposite inequality, the previously emitted outputs are supported on the inputs in P_k. By Eq. (14), they span a $2(k-1)$-dimensional symplectic subspace of the $2|P_k|$-dimensional phase space of the injected inputs. The rows of $S[F_k; P_k]$ are symplectically orthogonal to this subspace, since they correspond to outputs different from the emitted ones. They must therefore lie in its symplectic complement, whose dimension is $2|P_k| - 2(k-1)$. Hence, $\operatorname{rank} S[F_k; P_k] \leq 2|P_k| - 2(k-1)$, which proves the equality. □

Equation (16) depends only on the support sets defined in Eq. (5), not on the numerical values of the entries of S. Thus, the memory cost is determined by which outputs depend on which inputs. In particular, changing the squeezing parameters can change the entanglement across an emission cut without changing the memory cost, provided that the support pattern remains unchanged. The memory requirement therefore counts the number of qumodes that must be retained, rather than the amount of entanglement across the cut.

In practice, the cost is obtained by updating the running union $P_k = \bigcup_{j \leq k} \operatorname{supp}(o_j)$ and evaluating $|P_k| - k + 1$ at each step. This requires $O(\sum_k |\operatorname{supp}(o_k)|)$ time, which is linear in the size of the support data and involves no linear algebra.

IV. SEQUENTIAL GENERATION ALGORITHM

The target transformation S may be specified either as a symplectic matrix or as a Gaussian gate sequence. When only the symplectic matrix is available, the matrix-based protocol in Appendix A, discussed further in Sec. IV E, constructs the required in-register Gaussian operations and achieves the minimum memory cost given by Theorem 1. This section considers the second case, in which S is provided as a Gaussian gate sequence,

$$S = G_L \cdots G_1, \tag{17}$$

where each gate G_l acts on the set of qumodes $\mathrm{supp}(G_l)$. This is the natural representation for many applications, since bosonic encoding circuits and cluster-state constructions are usually specified as circuits rather than as symplectic matrices.

When a gate sequence is available, the Gaussian operations applied within the memory register can be taken directly from that sequence and scheduled according to the chosen emission order, without synthesizing new operations from S. The resulting protocol faithfully realizes the target transformation, although its memory usage need not attain the minimum given by Theorem 1.

A. Entanglement Structure of the Gate Sequence

The protocol is described in the Heisenberg picture. Each memory qumode is represented by a $2 \times 2N$ row block that expresses its two quadratures in terms of the input quadratures. When a qumode is injected, its row block is the identity on the corresponding input qumode. Here, $\mathrm{supp}(G_l)$ denotes the fixed set of qumodes on which the gate G_l acts directly. Applying G_l updates only the row blocks of the qumodes in $\mathrm{supp}(G_l)$, replacing them by linear combinations of those row blocks, while all other row blocks remain unchanged. These updated row blocks may already contain contributions from other input qumodes introduced through earlier entangling gates. Consequently, although G_l acts directly only on $\mathrm{supp}(G_l)$, its effect can propagate through the gate sequence and influence the final row blocks of additional qumodes.

This dependence is described by the entanglement support $E(q)$ of qumode q. It is defined as the smallest set of gate indices satisfying the following two conditions: It contains every l for which $q \in \mathrm{supp}(G_l)$, and whenever it contains l, it also contains every earlier index $l' < l$ such that $\mathrm{supp}(G_{l'}) \cap \mathrm{supp}(G_l) \neq \emptyset$. Thus, $E(q)$ contains all gates whose effects can propagate to q through the gate sequence. Any index set with this closure property is called support-closed. For an index set F, let Π_F denote the product of the gates $\{G_l : l \in F\}$ taken in the same order as in Eq. (17).

Lemma 1 (Locality of the entanglement support)**.** *Let F be support-closed and satisfy $F \supseteq E(q)$. Then the row pair of qumode q in Π_F is identical to its row pair in the full transformation S.*

Proof. The proof is by induction on the sequence length L. The statement is immediate for $L = 0$, since both transformations are the identity. Assume it holds for sequences of length $L-1$, and write $S = G_L \Pi'$, where $\Pi' = G_{L-1} \cdots G_1$.

If $q \notin \mathrm{supp}(G_L)$, then $L \notin E(q)$ and G_L does not change the row pair of q. The set $F \setminus \{L\}$ remains support-closed for the shortened sequence and contains the entanglement support of q in that sequence. The result then follows from the induction hypothesis.

If $q \in \mathrm{supp}(G_L)$, then $L \in E(q) \subseteq F$. In both S and

Algorithm 1 Sequential generation of S from a gate sequence

Definitions:
G_l: l-th gate in $S = G_L \cdots G_1$.
$\mathrm{supp}(G_l)$: qumodes acted on by G_l.
W: qumode labels reached by the reverse scan, initialized as $W = \{o_k\}$.
$\mathcal{C}$: ordered indices of unapplied gates selected by the scan.
$\mathcal{G}$: sequential operation sequence constructed by the algorithm.

Input:
Gate sequence $S = G_L \cdots G_1$.
Emission order $o_1, \ldots, o_N$.

Output:
Operation sequence $\mathcal{G}$ emitting outputs in the order $o_1, \ldots, o_N$.

$\mathcal{G} \leftarrow [\,]$
mark all G_l as unapplied
for $k = 1, \ldots, N$ **do**
  $W \leftarrow \{o_k\}$
  $\mathcal{C} \leftarrow [\,]$
  for $l = L, \ldots, 1$ with G_l unapplied **do**
    if $\mathrm{supp}(G_l) \cap W \neq \emptyset$ **then**
      prepend l to $\mathcal{C}$
      $W \leftarrow W \cup \mathrm{supp}(G_l)$
    end if
  end for
  for $l \in \mathcal{C}$ in increasing order **do**
    inject qumodes in $\mathrm{supp}(G_l)$ not yet in the register
    append these injections to $\mathcal{G}$
    apply G_l within the register
    mark G_l as applied
    append G_l to $\mathcal{G}$
  end for
  if o_k is not yet in the register **then**
    inject o_k
    append the injection to $\mathcal{G}$
  end if
  emit the memory qumode carrying o_k through a π full swap
  append the emission to $\mathcal{G}$
end for
return $\mathcal{G}$

Π_F, the gate G_L forms the row pair of q from the row pairs of the qumodes $q' \in \mathrm{supp}(G_L)$ immediately before the final gate. For each such q', its entanglement support in the shortened sequence is contained in $E(q) \setminus \{L\}$, and therefore in the support-closed set $F \setminus \{L\}$. By the induction hypothesis, the required row pairs of all such q' are the same in the two products. Applying the same gate G_L therefore gives the same row pair for q. □

B. Algorithm

Algorithm 1 follows the prescribed emission order. At step k, the reverse scan identifies the complete set of unapplied gates whose effects can propagate to the output o_k. The set W is initialized with o_k and enlarged whenever an unapplied gate acts on a qumode already in W, thereby tracing the dependence of o_k backward through the gate sequence. The selected gate indices are stored in $\mathcal{C}$. Although they are identified by a reverse scan, they are applied in increasing order, so their relative order is exactly the same as in the original gate sequence. A qumode is injected when it is first required by one of these gates.

After all gates in $\mathcal{C}$ have been applied, one memory qumode carries the complete output o_k. This qumode is emitted through a full swap. The in-register operation at step k is therefore the ordered product of the selected gates. Since these gates are taken directly from the given gate sequence, no additional synthesis of the in-register operation is required.

C. Correctness

Theorem 2 (Faithful realization from a gate sequence)**.** *Algorithm 1 applies every gate in Eq. (17) exactly once, emits o_k for each k, and faithfully realizes S. Each traveling qumode interacts with the register only once through a full swap, and every in-register operation is composed of gates from the original gate sequence.*

Proof. At every stage, the set of applied gates is support-closed, because it is enlarged only by adding complete entanglement supports. Marking the gates after application ensures that no gate is applied more than once.

Before the k-th emission, all gates in $E(o_k)$ have been applied. The reverse scan selects every unapplied gate whose action can influence o_k. Since every qumode is eventually emitted, every gate is eventually selected and therefore applied exactly once.

At the k-th emission, the applied gate set is support-closed and contains $E(o_k)$. By Lemma 1, the row pair of the memory qumode carrying o_k is therefore identical to the row pair of o_k in the full transformation S. The π full swap transfers this row pair exactly to the vacuum traveling qumode.

No later gate acts on an emitted qumode, since every gate affecting that qumode is applied before its emission. Previously emitted outputs therefore remain unchanged. After all N steps, the traveling qumodes carry all output row pairs of S, and the joint transformation is exactly S. □

The schedule is obtained in $O(NL)$ classical time, where N is the number of output qumodes and L is the number of gates in the input sequence. No matrix completion, factorization, or synthesis is required. Each of the original L Gaussian gates is applied exactly once.

D. Memory Usage and Optimality

The memory required by Algorithm 1 depends on the chosen gate sequence. A qumode enters the register when the first applied gate acts on it and remains there until its emission. Let r_k denote the number of memory qumodes in the register immediately before the k-th emission. The peak occupation is

$$w = \max_{1 \le k \le N} r_k, \tag{18}$$

which defines the entanglement width of the gate sequence for the chosen emission order.

Proposition 1 (Entanglement width versus the minimum)**.** *For any gate sequence realizing S and any emission order,*

$$r_k \ge \tfrac{1}{2} \operatorname{rank} S[F_k; P_k]$$

at every step. Consequently, $w \ge n_{\mathrm{mem}}(S)$. Both quantities can be computed in time polynomial in N and L, so the memory overhead of a given gate sequence can be determined before the protocol is executed.

Proof. By Theorem 2, the qumode emitted at step j carries the row pair of o_j in S, whose support is $\mathrm{supp}(o_j)$. An input can appear in this row pair only after that input has been injected. Therefore, by step k, the injected set must contain $P_k = \bigcup_{j \le k} \mathrm{supp}(o_j)$.

After $k-1$ outputs have been emitted, the register occupation equals the number of injected qumodes minus $k-1$. Hence,

$$r_k \ge |P_k| - (k-1) = \tfrac{1}{2} \operatorname{rank} S[F_k; P_k],$$

where the equality follows from Corollary 1. Taking the maximum over k gives $w \ge n_{\mathrm{mem}}(S)$.

The values r_k follow directly from the injection and emission times produced by the $O(NL)$ scheduling procedure, while $n_{\mathrm{mem}}(S)$ is obtained from the counting formula in Eq. (16). □

The difference $w - n_{\mathrm{mem}}(S)$ measures the additional memory introduced by the chosen gate sequence. At step k, the minimum required occupation is $|P_k| - (k-1)$, whereas Algorithm 1 retains every input qumode that has already been involved in an applied gate. Any input used

before the first emission that depends on it therefore contributes to the excess occupation. Such early injections may be caused by routing operations or by entanglement that is created and later removed within the circuit.

A gate sequence attains the minimum when no input qumode is introduced before the first output that depends on it. Whether this condition is satisfied can be determined by comparing w with $n_{\mathrm{mem}}(S)$ as described in Proposition 1.

E. The General Case

When a gate sequence is available, Algorithm 1 offers three practical advantages. First, the schedule can be constructed in $O(NL)$ time without any linear-algebra operations. Second, the in-register operations are taken directly from the original circuit, so the protocol uses exactly the L gates already specified. Third, the gate sequence determines the in-register operation applied before each emission, removing the freedom left open by the model in Sec. II.

If no gate sequence for S is known, or if the sequence has a nonzero memory overhead according to Proposition 1, the matrix-based protocol in Appendix A can be used instead. It takes only $S \in \mathrm{Sp}(2N,\mathbb{R})$ and an emission order as input, and realizes S with exactly $n_{\mathrm{mem}}(S)$ memory qumodes for any symplectic transformation. This is the explicit construction underlying the upper bound in Theorem 1.

The matrix-based protocol achieves optimal memory usage at the cost of additional synthesis. At each emission step, the target output o_k is first expressed in the basis of the qumodes currently stored in the register. The resulting conjugate pair is then extended to a full symplectic transformation by symplectic Gram–Schmidt completion, after which the qumode carrying o_k is emitted through a full swap. The complete procedure runs in $O(N^4)$ classical time.

The in-register operations are returned as general symplectic matrices T_k acting on at most $n_{\mathrm{mem}}(S)$ qumodes, rather than as sequences of elementary gates. Compiling each T_k using the Bloch–Messiah decomposition [20] described in Appendix A 4 requires $O(n_{\mathrm{mem}}^2)$ beam splitters and single-qumode squeezers per step, or $O(Nn_{\mathrm{mem}}^2)$ elementary gates over the full protocol. By comparison, Algorithm 1 applies the original L gates directly.

The matrix T_k is not unique. The protocol fixes only the conjugate pair that is to be emitted, while the remaining rows can be completed in different symplectic bases. This freedom affects the resulting gate decomposition, and the Gram–Schmidt construction generally couples all qumodes currently in the register. Finding the completion that minimizes the total elementary-gate count when only S is given remains an open problem.

After introducing the matrix-based protocol, a comparison with the gate-sequence protocol of Algorithm 1 clarifies their complementary input settings. When an encoding circuit is available, Algorithm 1 uses its original gate sequence without additional synthesis, although its memory usage need not be optimal. When only the target symplectic matrix S is available, the matrix-based protocol achieves the minimum memory cost but requires the synthesis of new in-register Gaussian operations. The comparison therefore highlights the tradeoff between reusing an existing circuit and minimizing the required memory.

TABLE I. Comparison of the gate-sequence protocol in Algorithm 1 and the matrix-based protocol in Algorithm 3 of Appendix A. Here L is the number of gates in the input sequence, and n_{mem} is the minimum memory requirement from Theorem 1. The gate-sequence protocol uses the original circuit gates directly, whereas the matrix-based protocol always achieves the minimum memory but requires synthesized, gauge-dependent in-register operations.

	Gate sequence	Matrix only
Input	$S = G_L \cdots G_1$	$S \in \mathrm{Sp}(2N,\mathbb{R})$
Memory qumodes	$\geq n_{\mathrm{mem}}$	n_{mem}
Classical runtime	$O(NL)$	$O(N^4)$
In-register operations	original circuit gates	synthesized
Elementary gates	L	$O(Nn_{\mathrm{mem}}^2)$

Table I summarizes the two protocols. For a given gate sequence, Proposition 1 determines whether its memory usage matches the minimum or whether the matrix-based protocol is preferable.

V. EMISSION-ORDER DEPENDENCE: THE CHAIN CODE

Theorem 1 determines the memory cost for any fixed emission order, but the order itself remains a design choice. This section examines its effect using a specific encoding circuit. For the same transformation S, different emission orders can change the required memory from a constant to the maximum value N.

A. The Chain Code

Consider a five-qumode one-dimensional encoding circuit consisting of one data qumode followed by four ancilla qumodes, as shown in Fig. 2. The input a_1 carries the data state, while $a_2,\ldots,a_5$ are ancilla qumodes prepared in GKP states. Neighboring qumodes are coupled by two-mode squeezing (TMS), as in GKP-stabilizer codes that encode one oscillator into several oscillators using TMS interactions with GKP ancilla qumodes [38, 39].

For the quadrature vector $(\hat{q}_j,\hat{p}_j,\hat{q}_{j+1},\hat{p}_{j+1})$, a TMS gate with squeezing parameter r is represented by

$$G(r) = \begin{pmatrix} \cosh r\, I & \sinh r\, Z \\ \sinh r\, Z & \cosh r\, I \end{pmatrix}, \qquad Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}, \quad (19)$$

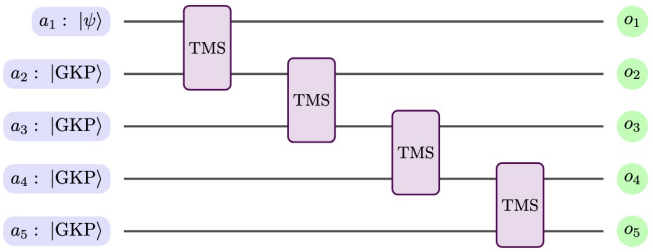

FIG. 2. Five-qumode chain encoder. The input qumode a_1 carries the data state $|\psi\rangle$, while $a_2, \ldots, a_5$ are GKP ancilla qumodes. Consecutive qumodes are coupled by nearest-neighbor TMS gates with squeezing parameter r. The corresponding output qumodes are labeled $o_1, \ldots, o_5$.

where I is the 2×2 identity matrix. The chain encoder applies this gate between consecutive qumodes,

$$S_{\text{chain}} = G_{N-1} \cdots G_2 G_1, \tag{20}$$

where G_j denotes $G(r)$ acting on qumodes j and $j+1$. Thus, the data qumode is first coupled to the first ancilla, which is then coupled to the next ancilla, and so on along the chain. The following analysis depends only on S_{chain}, not on the particular input states, as established in Sec. II.

The support of each output follows from the gate order in Eq. (20). Qumode k is acted on only by G_{k-1} and G_k, with G_0 and G_N absent. Its row pair becomes final after G_k for $k \leq N-1$, and after G_{N-1} for $k = N$. Since every block of Eq. (19) is nonzero for $r \neq 0$, the dependence on earlier inputs propagates along the chain:

$$\mathrm{supp}(o_k) = \begin{cases} \{a_1, \ldots, a_{k+1}\}, & k \leq N-1, \\ \{a_1, \ldots, a_N\}, & k = N. \end{cases} \tag{21}$$

Therefore, the final output depends on all input qumodes, while each earlier output depends only on the inputs up to one position beyond its own.

B. Two Emission Orders

Two natural choices are the forward order $o_1, o_2, \ldots, o_N$, which follows the chain, and the reverse order $o_N, o_{N-1}, \ldots, o_1$. Applying Eq. (8) to S_{chain} shows that these two orders have the largest possible difference in memory cost. The corresponding protocols for $N = 5$ are shown in Fig. 3.

For the forward order, Eq. (21) gives $P_k = \{a_1, \ldots, a_{k+1}\}$ for $k \leq N-1$. Corollary 1 therefore gives $\chi_k = \frac{1}{2} \operatorname{rank} S[F_k; P_k] = |P_k| - (k-1) = 2$ for $k \leq N-1$, while $\chi_N = 1$. Hence, $n_{\text{mem}} = 2$, independent of N. One memory qumode carries the output o_k being completed, while the other carries the boundary qumode $k+1$, through which the remaining gates retain access to the injected inputs.

For the reverse order, the first emitted output is o_N. Since $\mathrm{supp}(o_N) = \{a_1, \ldots, a_N\}$, all inputs must be injected before the first emission. Thus, $\chi_1 = N$, after which the register occupation decreases as $\chi_k = N - (k-1)$. The same transformation therefore requires only two memory qumodes in the forward order but N memory qumodes in the reverse order. For $N = 5$, the two occupation profiles are $(2, 2, 2, 2, 1)$ and $(5, 4, 3, 2, 1)$.

Algorithm 1 gives the corresponding gate-level protocols. In the forward order [Fig. 3(a)], the only unapplied gate needed to complete o_k is G_k. Each step therefore injects one new input qumode, applies one TMS gate, and emits one output. The protocol reaches a steady pattern with entanglement width $w = 2$, equal to the minimum.

In the reverse order [Fig. 3(b)], the entanglement support of the first output o_N contains the entire gate sequence. All N inputs and all $N-1$ TMS gates are therefore required before the first emission. The full encoding circuit is applied first, followed by the sequential release of all outputs, giving $w = N$. In both orders, the gate-sequence protocol attains the minimum for that order. The difference in memory cost is therefore caused entirely by the emission order.

C. The Order-selection Problem

The chain code shows that the emission order can change the memory cost of the same transformation from $O(1)$ to $\Theta(N)$, which is the largest possible variation. Choosing the emission order is therefore an important part of the protocol design.

Finding the best order is a discrete optimization problem over $N!$ possible permutations. However, the cost of any fixed order can be evaluated efficiently: Corollary 1 reduces it to a linear-time counting procedure. Exhaustive search is therefore practical only for small N. The next section introduces a heuristic that uses this efficient cost evaluation to select low-memory emission orders for larger systems.

VI. HEURISTIC EMISSION-ORDER SELECTION

The previous section introduced the problem of choosing the emission order. This section presents a deterministic greedy heuristic for an arbitrary $S \in \mathrm{Sp}(2N, \mathbb{R})$. The heuristic uses only the support sets of the outputs. Its performance is compared with the certified global optimum on a running example in this section and with coloring-based alternatives on a larger benchmark in Appendix B.

The output labels $o_1, \ldots, o_N$ are fixed by the transformation S; only the order in which these outputs are emitted is varied. This order is recorded by a permutation $\Xi = (\Xi_1, \ldots, \Xi_N)$ of $\{1, \ldots, N\}$, where Ξ_k is the label of the output emitted at step k. The sets in Eqs. (5) and (7)

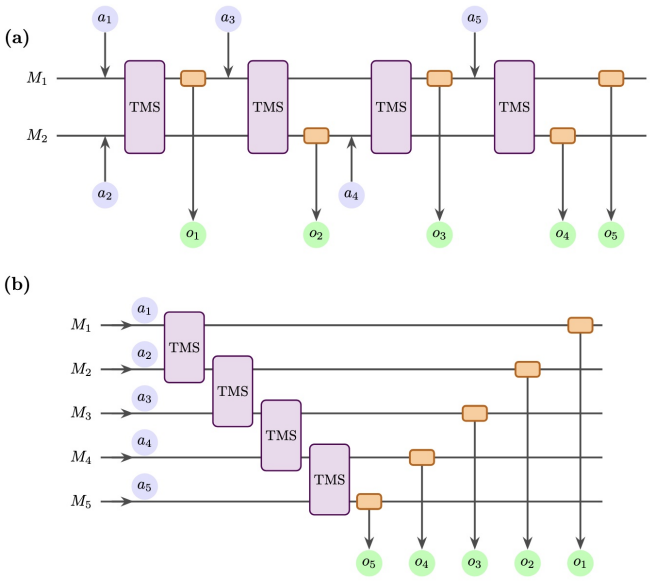

FIG. 3. Sequential emission of the $N = 5$ chain code in two different orders, generated by Algorithm 1. Horizontal lines denote memory qumodes $M_1, M_2, \ldots$, vertical arrows denote input injections, and the orange blocks denote π full swaps to traveling qumodes. (a) Forward order. Two memory qumodes are sufficient, giving $n_{\mathrm{mem}} = 2$. The first step injects a_1 and a_2; each subsequent step injects the next input into the memory qumode freed by the previous emission, applies one TMS gate, and emits the next output. The final step emits o_5 without an additional gate. (b) Reverse order. Since o_5 depends on all inputs, all five inputs and all four TMS gates are required before the first emission. The encoded outputs are then released sequentially, giving $n_{\mathrm{mem}} = 5$. Both panels realize the same transformation and differ only in the emission order.

are defined with respect to this order, and Corollary 1 gives the memory cost $n_{\mathrm{mem}}(\Xi) = \max_k \big(|P_k| - k + 1\big)$.

A. Greedy Minimum-frontier Selection

Algorithm 2 constructs the emission order one output at a time. At any step, R contains the outputs that have not yet been selected, while J contains the input qumodes already required by the selected outputs. If a remaining output o is emitted next, the additional input qumodes that must be injected are those in $\mathrm{supp}(o) \setminus J$.

By Corollary 1, minimizing the register occupation at the next step is therefore equivalent to minimizing $|\mathrm{supp}(o) \setminus J|$. The algorithm selects the output that requires the fewest new input qumodes, updates J, and repeats until all outputs have been ordered. Ties are resolved by the output labels, making the procedure deterministic.

After the order has been selected, the protocols in Sec. IV and Appendix A can be used to realize S with the corresponding memory cost.

Algorithm 2 Greedy emission-order selection

Definitions:
R: unselected outputs; J: required inputs; Ξ: emission order; c: maximum register occupation.

Input:
Symplectic matrix $S \in \mathrm{Sp}(2N, \mathbb{R})$.

Output:
Emission order Ξ and memory cost $c = n_{\mathrm{mem}}(\Xi)$.

compute $\mathrm{supp}(o)$ for every output o
$R \leftarrow \{o_1, \ldots, o_N\}$
$J \leftarrow \emptyset$
$\Xi \leftarrow [\,]$
$c \leftarrow 0$
while $R \neq \emptyset$ **do**
  $o^* \leftarrow \arg\min_{o \in R} |\mathrm{supp}(o) \setminus J|$ ▷ *Break ties by output label*
  append o^* to Ξ
  $J \leftarrow J \cup \mathrm{supp}(o^*)$
  $R \leftarrow R \setminus \{o^*\}$
  $c \leftarrow \max(c, |J| - |\Xi| + 1)$
end while
return Ξ, c

B. Complexity

Algorithm 2 requires only set operations. If J is stored as a boolean array, evaluating a candidate output o takes $O(|\mathrm{supp}(o)|)$ time. At a given step, evaluating all remaining outputs therefore costs $O\big(\sum_{o \in R} |\mathrm{supp}(o)|\big)$. Over all N steps, the total runtime is

$$O\left(N \sum_{o} |\mathrm{supp}(o)|\right) \leq O(N^2 s), \tag{22}$$

where $s = \max_o |\mathrm{supp}(o)|$ is the largest output support. No linear-algebra operations are required.

C. Example: The Analog Shor Code

The greedy heuristic is evaluated on the continuous-variable analog of the nine-qubit Shor code [32, 40], whose encoding circuit is shown in Fig. 4. The data state is assigned to qumode 1, while qumodes $2, \ldots, 9$ contain the resource states.

The memory cost depends strongly on the emission order. Emitting the outputs in the labeling order $o_1, o_2, \ldots, o_9$ requires $n_{\mathrm{mem}} = 5$ memory qumodes. The exact optimum over all emission orders is $n_{\mathrm{mem}} = 3$, obtained by a dynamic program over subsets of emitted outputs with runtime $O(2^N \mathrm{poly}(N))$. Among 20 000 uniformly sampled random orders, only 1.6% achieve cost 3. The most frequent cost is 5, and the largest sampled cost is 7.

For this encoder, Algorithm 2 reaches the certified op-

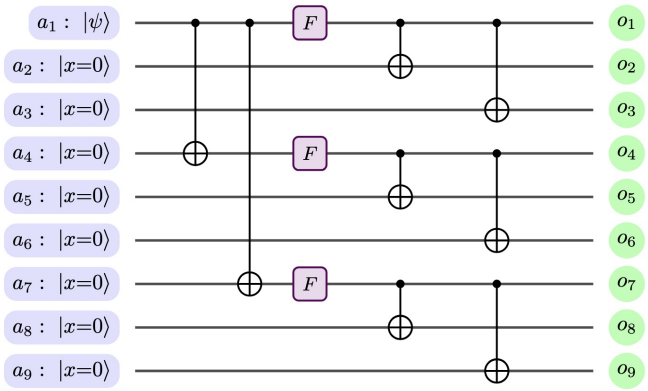

FIG. 4. Encoding circuit of the nine-qumode analog Shor code. The input qumode a_1 carries the data state $|\psi\rangle$, while $a_2, \ldots, a_9$ are initialized in the position eigenstate $|x = 0\rangle$. The circuit consists of Fourier gates F and SUM gates, and the corresponding output qumodes are labeled $o_1, \ldots, o_9$.

timum and returns

$$\Xi = (5,\ 6,\ 4,\ 2,\ 1,\ 3,\ 8,\ 7,\ 9), \tag{23}$$

with occupation profile $(2, 2, 2, 3, 3, 2, 2, 2, 1)$ and $n_{\mathrm{mem}}(\Xi) = 3$. The corresponding emission circuit generated by Algorithm 1 is shown in Fig. 5.

The greedy order follows the hierarchical structure of the encoder and processes its three-qumode blocks one at a time. During each block, one memory qumode retains the data qumode, a second retains the central qumode of the block, and a third is used to complete and emit the other two qumodes in sequence. This structure explains why three memory qumodes are sufficient.

D. Guarantees and Limitations

Algorithm 2 minimizes the register occupation at each individual step. However, the cost of an emission order is determined by the largest occupation over the entire sequence, so a choice that is optimal locally may lead to a larger cost at a later step. The heuristic therefore does not guarantee a globally optimal order. The computational complexity of finding the exact optimal emission order also remains open.

The quality of the greedy solution can still be assessed in practice. Its memory cost is evaluated exactly using Corollary 1 and can be compared efficiently with randomly sampled orders. For moderate N, the result can also be compared with the exact optimum obtained by a subset dynamic program based on the Bellman–Held–Karp approach [41, 42].

An alternative strategy, inspired by register-allocation techniques in classical compilers [43], is to order the emissions by graph-coloring heuristics on a conflict graph derived from the structure of the Gaussian transformation. Appendix B compares Algorithm 2 with four such coloring-based heuristics on a benchmark of 450 random Gaussian transformations with certified optima. The coloring-based orders recover the optimum on fewer instances than Algorithm 2, because they rank the outputs using degree-based proxy metrics, whereas Algorithm 2 directly tracks the set of injected inputs J, which determines the actual register occupation.

VII. MEMORY SCALING FOR LOCALLY STRUCTURED TRANSFORMATIONS

The preceding sections showed that the memory cost depends strongly on the emission order and developed methods for selecting suitable orders for individual encoders. A broader question is how the minimum memory scales across families of transformations as the system size increases.

Corollary 1 shows that the memory cost is determined entirely by the output supports defined in Eq. (5). For a generic transformation S, every output depends on every input. In that case, all N inputs must be injected before the first emission, and N memory qumodes are required for any emission order. A smaller memory register is therefore possible only when the supports are sparse.

In many physically relevant settings, this sparsity arises from locality. For cluster-state transformations defined on locally connected graphs, each output depends only on inputs within a local neighborhood [44, 45]. This section shows that, for such transformations, the required memory scales with the size of the boundary between the emitted and unemitted regions rather than with the total number of qumodes. The scaling is independent of the type, number, and strength of the couplings. It is achieved by a simple sweep through the structure, without any search over emission orders.

A. Slice-local Transformations

Partition the N qumodes into slices $V_1, \ldots, V_m$, and let $v(q)$ denote the index of the slice containing qumode q. The transformation S is called slice-local with range ρ if

$$|v(a) - v(o)| \le \rho \tag{24}$$

for every output o and every input $a \in \mathrm{supp}(o)$. Thus, each output depends only on inputs located within ρ slices of its own slice. The slice order emits all outputs in V_1 first, followed by those in V_2, and so on; the order within each slice is arbitrary.

Theorem 3 (Memory bound for slice-local transformations)**.** *Let $S \in \mathrm{Sp}(2N, \mathbb{R})$ be slice-local with range ρ with respect to the slices $V_1, \ldots, V_m$. Under the slice order,*

$$n_{\mathrm{mem}} \le (\rho + 1) \max_i |V_i|. \tag{25}$$

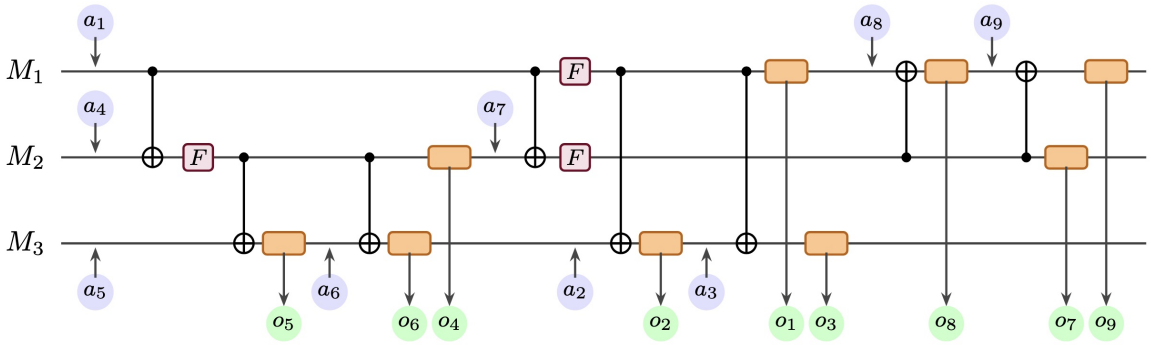

FIG. 5. Emission circuit for the analog Shor code in the greedy emission order of Eq. (23), generated by Algorithm 1. The circuit proceeds from left to right. The horizontal lines represent the three memory qumodes M_1, M_2, M_3, and the vertical arrows labeled $a_1, \ldots, a_9$ indicate input injections. A SUM gate is represented by a control dot and a target $\oplus$, while F denotes the Fourier gate. Each orange block represents a π full swap between a memory qumode and a vacuum traveling qumode. The traveling qumode is then emitted as the corresponding output o_k, indicated by a downward arrow. In the circuit shown, the emission operations are distributed among different memory qumodes. Nevertheless, only one memory qumode needs to support controlled emission into the traveling channel, since additional SWAP gates within the register can route each output state to that memory qumode before emission.

Proof. Consider the k-th emission, and let $r = v(o_k)$ be the slice containing o_k. Under the slice order, all outputs emitted up to this step belong to $V_1, \ldots, V_r$. By Eq. (24), their supports extend no further than ρ slices beyond V_r. Therefore,

$$P_k = \bigcup_{j \le k} \mathrm{supp}(o_j) \subseteq V_1 \cup \cdots \cup V_{\min(r+\rho,m)}. \tag{26}$$

Before the k-th emission, all outputs in $V_1, \ldots, V_{r-1}$ have already been emitted, so $k - 1 \ge \sum_{i=1}^{r-1} |V_i|$. Using Corollary 1, $\chi_k = |P_k| - (k-1) \le \sum_{i=r}^{\min(r+\rho,m)} |V_i| \le (\rho+1) \max_i |V_i|$. Taking the maximum over all emission steps proves Eq. (25). □

B. Graph-local Transformations

Graphs provide a natural class of slice-local transformations. A transformation S is called graph-local on a graph G if

$$\mathrm{supp}(o) \subseteq \{o\} \cup \mathcal{N}(o) \quad \text{for every output } o, \tag{27}$$

where $\mathcal{N}(o)$ denotes the set of neighbors of o in G. Thus, each output depends only on its own input and on the inputs associated with adjacent vertices.

Corollary 2 (Graph-local transformations)**.** *Let S be graph-local on G, and partition the vertices into slices $V_1, \ldots, V_m$ such that every edge connects vertices in the same slice or in adjacent slices. Then S is slice-local with range $\rho = 1$, and the slice order satisfies*

$$n_{\mathrm{mem}} \le 2 \max_i |V_i|.$$

For a D-dimensional cubic lattice with linear size ℓ and $N = \ell^D$ qumodes, sliced along one axis,

$$n_{\mathrm{mem}} \le 2\ell^{D-1} = 2N^{(D-1)/D}. \tag{28}$$

This condition includes continuous-variable cluster-state transformations [8, 9], for which each output depends only on its own input and those of neighboring vertices. It also allows diagonal, decorated, or irregular coupling patterns, provided that every coupling connects qumodes in the same slice or in adjacent slices. The bound depends only on this support pattern, not on the form or strength of the interactions.

Figure 6 illustrates the slice order in one and two dimensions. The emission proceeds slice by slice, while the memory register retains only the boundary between the emitted and unemitted regions, together with the qumode currently being completed.

C. Tightness and Significance

For cluster-state transformations defined on locally connected graphs, the slice order provides a natural sequential implementation whose memory cost is determined by the corresponding support structure.

Proposition 2 (Slice-order cost on cubic lattices)**.** *Consider the cluster-state transformation on a D-dimensional cubic lattice with nearest-neighbor connectivity and $N = \ell^D$ qumodes, where each lattice edge represents a controlled-Z interaction. For a slice order taken along one lattice axis,*

$$n_{\mathrm{mem}} = \ell^{D-1} + 1 \tag{29}$$

for every lattice linear size ℓ and for any emission order within each slice.

Proof. Consider the emission of the c-th output in slice V_r, where $2 \le r < m$. At this step, all outputs in $V_1, \ldots, V_{r-1}$ and $c-1$ outputs in V_r have already been

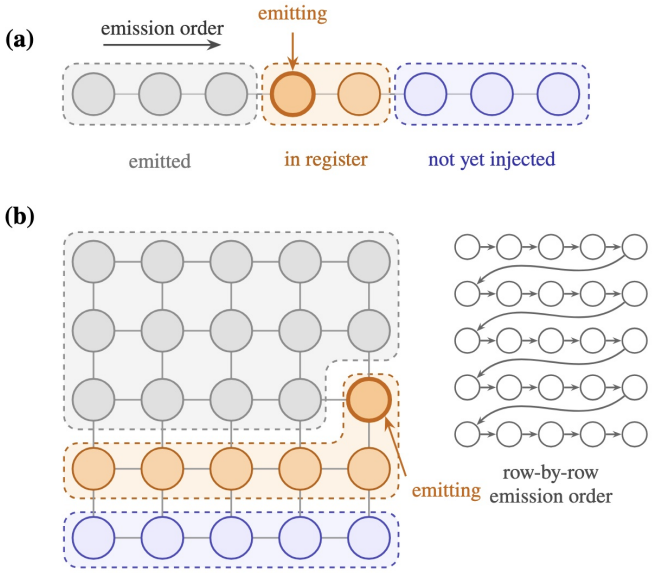

FIG. 6. Emission front for graph-local transformations at one step of the slice order. The dashed boxes indicate emitted qumodes (gray), qumodes currently held in the memory register (orange), and qumodes not yet injected (blue). The qumode with the thick outline is the one being emitted. (a) For a one-dimensional chain, each slice contains one qumode, and the outputs are emitted sequentially along the chain. At the stage shown, two qumodes are held in the memory register. (b) For a two-dimensional lattice of width ℓ, each row forms one slice. The slices are processed row by row, with the emission order illustrated on the right. At the stage shown, the memory register contains the qumode being emitted together with the injected row ahead of the emission front, for a total of $\ell + 1$ memory qumodes.

emitted. The injected set contains $V_1, \ldots, V_r$. In particular, since all outputs in V_{r-1} have already been emitted and collectively depend on all inputs in the adjacent slice V_r, every input in V_r must already have been injected. The injected set also contains the c inputs in V_{r+1} that are adjacent to the first c outputs emitted from V_r.

Hence, the number of injected inputs is $r\ell^{D-1}+c$, while the number of previously emitted outputs is $(r-1)\ell^{D-1}+c-1$. Corollary 1 therefore gives $\chi_k = \ell^{D-1}+1$, independently of r, c, and the emission order within the slice. During the first slice, the occupation increases up to this value, while during the final slice it decreases below it. This proves Eq. (29). □

These results establish the following scaling behavior for locally connected structures. On a D-dimensional cubic lattice with $N = \ell^D$ qumodes, the memory required by the slice order scales as $O(\ell^{D-1}) = O(N^{(D-1)/D})$. In particular, this scaling is constant in one dimension and $O(\sqrt{N})$ in two dimensions. More generally, the memory grows with the size of the boundary between the emitted and unemitted regions rather than with the total number of qumodes.

The slice order discussed above emits one output at a time. Although this minimizes the number of simultaneously active emission channels, the total generation time still grows with the number of outputs. A natural way to shorten this time is to allow several outputs to be emitted in parallel. Such parallelization can be implemented in two ways. One approach uses a single memory register equipped with multiple emission heads, so that several outputs can be released simultaneously from different memory qumodes. The other uses multiple memory registers, each with its own emission head, and distributes the generation process among the registers. Both approaches reduce the number of sequential emission steps. However, multiple emission heads within a shared register can reuse part of the stored information and therefore require only a moderate increase in memory, whereas multiple independent registers duplicate part of the memory associated with the emission front. Consequently, when simultaneous release from several memory qumodes is experimentally available, parallel emission within a single register provides a more memory-efficient tradeoff between generation time and hardware resources.

A similar slice-by-slice generation structure appears in time-multiplexed optical experiments, where two-dimensional cluster states are generated by retaining qumodes in delay lines while earlier outputs are emitted [12, 13]. These experiments prepare specific cluster states from fixed squeezed-state inputs. In contrast, Theorem 3 applies to the full Gaussian transformation and therefore to arbitrary input states. It also applies to any coupling pattern satisfying the locality condition, while Eq. (8) gives the exact memory cost for a specified emission order.

VIII. CONCLUSION AND OUTLOOK

This work establishes the optimal memory cost of sequentially realizing a multimode Gaussian transformation. For any $S \in \mathrm{Sp}(2N, \mathbb{R})$ and any fixed emission order, the minimum number of memory qumodes is given by Eq. (8). Corollary 1 reduces this rank expression to the number of input qumodes injected so far minus the number of outputs already emitted. The memory cost therefore depends only on the support pattern of S and can be evaluated in time linear in the size of the support data.

The minimum memory cost for an arbitrary symplectic matrix is achieved by the matrix-based protocol in Appendix A. When a gate sequence is available, Algorithm 1 instead constructs the sequential implementation directly from the original gates. Its memory usage need not attain the minimum, because the given gate decomposition may not be the most memory-efficient realization of the same transformation. The emission order is also an important design choice, since different orders can require substantially different numbers of memory qumodes for the same gate sequence. To address this ordering prob-

lem, Sec. VI introduces a greedy algorithm that selects the output requiring the fewest new input qumodes at each step and generally produces memory-efficient emission orders. For transformations with local support on a D-dimensional cubic lattice of N qumodes, the memory grows only with the size of the boundary between the emitted and unemitted regions, giving $O(N^{(D-1)/D})$ scaling.

Although the implemented transformations are Gaussian, the protocols do not assume Gaussian input states and therefore also apply to non-Gaussian inputs, including GKP and cat states. Since such states provide the non-Gaussian resources required for universal continuous-variable quantum computation, the proposed framework offers a resource-efficient and explicit scheme for communication between modules in modular architectures for universal quantum computation.

Several questions remain open. For qubit graph states, optimizing the photon emission order to minimize the number of emitters is NP-hard [31]. Whether or not optimizing the emission order of an arbitrary Gaussian transformation to minimize the required number of memory qumodes is also NP-hard remains unknown. For locally connected lattice families, characterizing how the minimum memory cost depends on the lattice geometry and emission order also remains an open problem. In the matrix-based protocol, the symplectic completion used to construct the in-register operations is generally not unique, and the resulting symplectic matrices can admit many gate decompositions. Selecting the completions and decompositions that minimize the total number of beam splitters and single-qumode squeezers is another open problem. Finally, the present analysis assumes ideal operations. Extending it to include memory decay, imperfect full swaps, and other hardware errors is necessary for a complete assessment of sequential Gaussian implementations.

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Appendix A: Sequential Generation from the Symplectic Matrix

This appendix considers the case in which the target transformation is specified only by a symplectic matrix $S \in \mathrm{Sp}(2N, \mathbb{R})$, with no gate sequence available. An explicit algorithm is given that realizes S faithfully under sequential emission by single full swaps while using exactly $n_{\mathrm{mem}}(S)$ memory qumodes, for any symplectic S and any emission order. This construction provides the upper bound in Theorem 1 and can be used whenever no gate sequence is known or when the entanglement width of a known sequence exceeds $n_{\mathrm{mem}}(S)$.

Unlike Algorithm 1, the in-register operations cannot be taken directly from a circuit and must instead be constructed from S. At each step, the next output is expressed in the basis of the qumodes currently stored in the register. This expression is then extended to a full symplectic operation on the register, after which the corresponding qumode is emitted. All steps are obtained from explicit linear-algebra operations.

1. Heisenberg Representation

The algorithm is formulated in the Heisenberg picture. If the register contains m memory qumodes, their quadratures are collected in a matrix $M \in \mathbb{R}^{2m\times 2N}$. Each qumode contributes a $2\times 2N$ row pair expressing its two quadratures in terms of the $2N$ input quadratures.

Because the stored qumodes satisfy the canonical commutation relations,

$$M\Omega M^{\top} = \Omega_m, \qquad \Omega_m = \bigoplus_{j=1}^{m} \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix}. \tag{A1}$$

Injecting an input qumode appends its identity row pair to M. An in-register Gaussian operation acts as $M \mapsto TM$, with T symplectic with respect to Ω_m, and therefore preserves Eq. (A1). Emission removes one conjugate row pair, leaving a symplectic frame for the remaining $m-1$ qumodes.

The construction uses two earlier results: Different output qumodes commute by Eq. (14), and all inputs required for o_k have been injected by step k because $\mathrm{supp}(o_k) \subseteq P_k$.

2. Algorithm

At step k, Algorithm 3 first injects any input qumodes in $\mathrm{supp}(o_k)$ that are not yet present in the register. It then constructs an in-register symplectic operation that places the output qumode o_k on the first memory qumode.

Let $\alpha = S[o_k, :]$ denote the row pair of o_k in the input quadratures. Since the current memory qumodes are represented by the rows of M, a matrix $A \in \mathbb{R}^{2\times 2m}$ satisfying $\alpha = AM$ expresses o_k in the coordinates of the register. Lemma 2 shows that this matrix is unique and is given by $A = \alpha\Omega M^{\top}\Omega_m^{-1}$. The same lemma shows that the two rows of A form a normalized conjugate pair with respect to Ω_m.

The subroutine $\mathrm{Complete}(A, \Omega_m)$ extends this pair to a full symplectic matrix. Starting from the pair (q, p) given by the two rows of A, each additional vector v is made

Algorithm 3 Sequential generation of S from its symplectic matrix

Definitions:
Mem: row-pair representations of the current memory qumodes.
Injected: input qumodes already injected.
$M = \mathrm{stack}(\mathrm{Mem})$: register matrix.
e_a: identity row pair of input qumode a.
$\alpha = S[o_k, :]$: row pair of output qumode o_k.
$\mathcal{G}$: constructed operation sequence.

Input:
Symplectic matrix $S \in \mathrm{Sp}(2N, \mathbb{R})$.
Emission order $o_1, \ldots, o_N$.

Output:
Operation sequence $\mathcal{G}$ emitting outputs in the order $o_1, \ldots, o_N$.

$\mathcal{G} \leftarrow [\,]$
Mem $\leftarrow [\,]$
Injected $\leftarrow \emptyset$
for $k = 1, \ldots, N$ **do**
  for $a \in \mathrm{supp}(o_k) \setminus$ Injected **do**
    append e_a to Mem
    Injected $\leftarrow$ Injected $\cup \{a\}$
    append inject(a) to $\mathcal{G}$
  end for
  $m \leftarrow |\mathrm{Mem}|$
  $M \leftarrow \mathrm{stack}(\mathrm{Mem})$
  $\alpha \leftarrow S[o_k, :]$
  $A \leftarrow \alpha \Omega M^\top \Omega_m^{-1}$ ▷ $\alpha = AM$
  $T \leftarrow \mathrm{Complete}(A, \Omega_m)$ ▷ $T[1{:}2] = A$
  $M \leftarrow TM$
  append T to $\mathcal{G}$
  $f_k \leftarrow M[1{:}2, :]$
  emit f_k through a π full swap
  append the emission to $\mathcal{G}$
  Mem $\leftarrow$ row pairs of M after removing the first qumode
end for
return $\mathcal{G}$

symplectically orthogonal to the previously selected pairs using

$$v \mapsto v - \{v, p\}_{\Omega_m} q + \{v, q\}_{\Omega_m} p. \tag{A2}$$

The remaining vectors are then paired and normalized until a matrix $T \in \mathbb{R}^{2m \times 2m}$ is obtained with $T\Omega_m T^\top = \Omega_m$ and $T[1{:}2] = A$.

After all gates in $\mathcal{C}$ have been applied, one memory qumode carries the complete output o_k. This qumode is then emitted through a full swap. The in-register operation at step k is therefore obtained by taking the selected gates directly from the original circuit while preserving their original relative order. Equivalently, it is the ordered subsequence of the original gate sequence specified by $\mathcal{C}$. Hence, neither the gate content nor the gate ordering needs to be resynthesized.

3. Correctness

Lemma 2 (Separability). *At step k, the output row pair $\alpha = S[o_k, :]$ lies in the row space of M. Therefore, there is a unique matrix A such that $\alpha = AM$. Moreover, $A\Omega_m A^\top = \left(\begin{smallmatrix} 0 & 1 \\ -1 & 0 \end{smallmatrix}\right)$.*

Proof. Since $\mathrm{supp}(o_k) \subseteq P_k$ by Eqs. (5) and (7), the row pair $\alpha = S[o_k, :]$ depends only on inputs that have already been injected.

The phase space of the injected inputs is spanned by the previously emitted output qumodes and the qumodes remaining in the register. Each emission removes one output row pair, while the remaining register qumodes commute with that output. By Eq. (14), o_k also commutes with every previously emitted output. Hence, α has no component along the removed output pairs and must lie in the row space of M.

Because M has full row rank, the solution to $\alpha = AM$ is unique. Using Eq. (A1), $A = \alpha \Omega M^\top \Omega_m^{-1}$. Finally, $A\Omega_m A^\top = (AM)\Omega(AM)^\top = \alpha\Omega\alpha^\top = \left(\begin{smallmatrix} 0 & 1 \\ -1 & 0 \end{smallmatrix}\right)$ by Eq. (14). Thus, the rows of A form a normalized conjugate pair, and the symplectic completion is well defined. □

Lemma 3 (Clean emission). *After the update $M \leftarrow TM$, the first memory qumode carries the output o_k. Emitting this qumode through a full swap preserves the information already stored in the register for all later outputs.*

Proof. By construction, $T[1{:}2] = A$. Therefore, the first row pair of TM is $AM = \alpha = S[o_k, :]$, so the first memory qumode carries the complete output o_k.

Since T is invertible, the update $M \mapsto TM$ changes only the symplectic basis of the register and leaves its row space unchanged. Consider a later output $o_{k'}$ with $k' > k$. By Eq. (14), $o_{k'}$ is symplectically orthogonal to o_k. The part of $o_{k'}$ supported on inputs not yet injected is also symplectically orthogonal to o_k, because o_k is supported only on inputs already present in the register. It follows that the component of $o_{k'}$ currently stored in the register is symplectically orthogonal to the first row pair of TM.

The remaining rows of TM span the symplectic complement of this first row pair within the register. Removing the first memory qumode therefore preserves all information currently stored for the later emissions. The full swap transfers o_k to the vacuum traveling qumode and completes the emission. □

Theorem 4 (Faithful realization at the minimum). *Algorithm 3 emits $f_k = o_k$ at every step and therefore realizes S faithfully. Each traveling qumode interacts with the register only once through a full swap. The peak register occupation is $n_{\mathrm{mem}}(S) = \max_k \frac{1}{2} \operatorname{rank} S[F_k; P_k]$.*

Proof. Lemmas 2 and 3 imply that the k-th traveling qumode carries the output row pair o_k. After all N emissions, the traveling qumodes therefore carry all output

row pairs of S, so the resulting transformation is exactly S.

The in-register symplectic operations do not change the number of qumodes. The register size increases only when an input is injected and decreases only when an output is emitted. Immediately before the k-th emission, the injected set is exactly P_k, and $k-1$ outputs have already been emitted. The register therefore contains $|P_k| - (k-1)$ memory qumodes. By Corollary 1, this equals $\frac{1}{2}\operatorname{rank} S[F_k; P_k]$. Taking the maximum over k gives $n_{\mathrm{mem}}(S)$, so Algorithm 3 achieves the minimum. □

4. Complexity and Compilation

At step k, the matrix $A = \alpha\Omega M^\top \Omega_m^{-1}$ is computed in $O(Nm)$ time. The symplectic completion and the update $M \leftarrow TM$ require $O(m^3)$ and $O(m^2N)$ time, respectively. Since $m \le n_{\mathrm{mem}}(S) \le N$, each step costs at most $O(N^3)$, and the full algorithm runs in $O(N^4)$ time.

Algorithm 3 returns each in-register operation as a symplectic matrix T_k acting on at most $n_{\mathrm{mem}}(S)$ memory qumodes. This matches the model of Sec. II, where arbitrary Gaussian operations within the register are assumed to be available. To implement T_k using elementary gates, two choices must be considered: the symplectic completion used to construct T_k, and the decomposition of the resulting matrix into hardware operations.

The protocol fixes only the first row pair of T_k, $T_k[1{:}2] = A$, which places the output o_k on the first memory qumode. The remaining rows may be chosen in any way that makes T_k symplectic. Different choices produce the same emitted output and use the same number of memory qumodes, but may lead to different elementary gate counts. The subroutine Complete selects one such completion using symplectic Gram–Schmidt orthogonalization against the standard basis. This construction generally couples all qumodes currently held in the register. When a gate sequence is available, Algorithm 1 avoids this choice by taking the in-register operations directly from the given sequence.

For a fixed T_k, the Bloch–Messiah decomposition gives

$$T_k = O_{\mathrm{out}} \left[\bigoplus_j \mathrm{Sq}(r_j) \right] O_{\mathrm{in}}, \tag{A3}$$

where O_{in} and O_{out} are passive interferometers and $\mathrm{Sq}(r_j)$ denotes single-qumode squeezing. The passive interferometers can be decomposed into beam-splitter networks using either the triangular [46] or rectangular [47] construction. Computing the Bloch–Messiah decomposition costs $O(m^3)$ time. The resulting circuit contains $m(m-1)$ beam splitters and m single-qumode squeezers, giving a total elementary-gate count of $O(Nn_{\mathrm{mem}}^2)$ over all emission steps.

The elementary-gate count depends on the chosen symplectic completion. Further reductions may also be possible by commuting, merging, or canceling gates across successive steps, although methods developed for qubit circuits [48, 49] do not directly apply to beam splitters and single-qumode squeezers. Determining the minimum elementary-gate count from S alone remains open. This freedom affects only the compilation cost, while the minimum number of memory qumodes remains fixed by Eq. (8).

Appendix B: Benchmark Comparison with Coloring-Based Emission Orders

This appendix compares Algorithm 2 with emission-order heuristics inspired by graph-coloring-based register allocation [43]. The comparison uses a benchmark of 450 random Gaussian transformations on $N = 12$ qumodes, generated from a fixed seed and divided into three families of 150 instances each. In the sparse random family, the number of gates is drawn uniformly from the integers in $[N, 2N]$, and each gate acts on a pair of distinct qumodes drawn uniformly at random from all pairs, with repeated pairs permitted. In the random tree family, the qumodes are placed in a uniformly random order, and each qumode after the first is coupled to one uniformly chosen earlier qumode, giving $N-1$ gates that form a tree. The application order of these gates is then randomized. In the brickwork family, the qumodes are arranged on a line and the gates form alternating layers of nearest-neighbor pairs, shifted by one qumode between consecutive layers. The number of layers is one, two, or three with probabilities 0.1, 0.45, and 0.45, respectively, and each potential gate is included independently with probability 0.8. Every gate is a generic two-mode Gaussian gate, and the output supports are obtained by propagating the supports through the gate list.

For every instance, the exact minimum memory cost over all emission orders is certified by the Bellman–Held–Karp dynamic program [41, 42]. The system size $N = 12$ is chosen so that this certification remains feasible for all 450 instances.

The coloring-based heuristics operate on a conflict graph whose vertices are the outputs. The next output to emit is the remaining vertex of minimum degree, or minimum weighted degree in the weighted variants. The degrees are recomputed after each selection, and ties are broken by output label. Two graph constructions are considered. In the support-overlap graph, two outputs are adjacent when their supports intersect, and the weighted variant assigns the edge between o_i and o_j the weight $|\mathrm{supp}(o_i) \cap \mathrm{supp}(o_j)|$. In the gate graph, outputs o_i and o_j are adjacent when at least one gate in the circuit couples qumodes i and j, and the weighted variant assigns to each edge a weight equal to the number of such gates.

Table II reports, for each heuristic, the number of instances on which the resulting memory cost exceeds the certified optimum by at most a given number of qumodes.

TABLE II. Cumulative excess over the certified optimum on the 450-instance benchmark. The column labeled x gives the number of instances on which the heuristic uses at most x memory qumodes more than the exact minimum. The last column gives the largest excess.

	Excess $\leq x$					
Method	0	1	2	3	4	Worst
Algorithm 2	313	424	447	450	450	+3
Support overlap, weighted	127	281	416	447	450	+4
Support overlap, unweighted	70	172	285	390	434	+7
Gate graph, unweighted	150	196	267	350	414	+7
Gate graph, weighted	131	176	266	350	415	+7

Algorithm 2 attains the optimum on 313 of the 450 instances, uses at most one additional memory qumode on 424 instances, and never exceeds the optimum by more than three. The best-performing coloring variant, the weighted support-overlap graph, attains the optimum on 127 instances and exceeds it by up to four. The unweighted gate graph attains the optimum on 150 instances, more than either support-overlap variant, but its excess reaches seven qumodes, and 36 of its orders exceed the optimum by five or more. The advantage of Algorithm 2 persists within each family, i.e., it is optimal on 108 of 150 sparse instances, 57 of 150 tree instances, and 148 of 150 brickwork instances, in each case more than any coloring variant.

The comparison indicates why the greedy rule outperforms the coloring-based orders. The degree of a vertex in a conflict graph is only an indirect proxy for the memory pressure associated with an output. By Corollary 1, the register occupation is determined exactly by the number of injected inputs, and Algorithm 2 minimizes this quantity directly at every step. The coloring-based orders optimize the proxy rather than the occupation itself, which leads to heavier tails in the excess distribution.

[1] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim, Phys. Rev. A **89**, 022317 (2014).
[2] N. H. Nickerson, J. F. Fitzsimons, and S. C. Benjamin, Phys. Rev. X **4**, 041041 (2014).
[3] H. J. Kimble, Nature **453**, 1023 (2008).
[4] S. Wehner, D. Elkouss, and R. Hanson, Science **362**, eaam9288 (2018).
[5] M. Reagor, W. Pfaff, C. Axline, R. W. Heeres, N. Ofek, K. Sliwa, E. Holland, C. Wang, J. Blumoff, K. Chou, M. J. Hatridge, L. Frunzio, M. H. Devoret, L. Jiang, and R. J. Schoelkopf, Phys. Rev. B **94**, 014506 (2016).
[6] W. Pfaff, C. J. Axline, L. D. Burkhart, U. Vool, P. Reinhold, L. Frunzio, L. Jiang, M. H. Devoret, and R. J. Schoelkopf, Nat. Phys. **13**, 882 (2017).
[7] C. J. Axline, L. D. Burkhart, W. Pfaff, M. Zhang, K. Chou, P. Campagne-Ibarcq, P. Reinhold, L. Frunzio, S. M. Girvin, L. Jiang, M. H. Devoret, and R. J. Schoelkopf, Nat. Phys. **14**, 705 (2018).
[8] N. C. Menicucci, P. van Loock, M. Gu, C. Weedbrook, T. C. Ralph, and M. A. Nielsen, Phys. Rev. Lett. **97**, 110501 (2006).
[9] N. C. Menicucci, Phys. Rev. Lett. **112**, 120504 (2014).
[10] S. Yokoyama, R. Ukai, S. C. Armstrong, C. Sornphiphatphong, T. Kaji, S. Suzuki, J.-i. Yoshikawa, H. Yonezawa, N. C. Menicucci, and A. Furusawa, Nat. Photonics **7**, 982 (2013).
[11] J.-i. Yoshikawa, S. Yokoyama, T. Kaji, C. Sornphiphatphong, Y. Shiozawa, K. Makino, and A. Furusawa, APL Photonics **1**, 060801 (2016).
[12] W. Asavanant, Y. Shiozawa, S. Yokoyama, B. Charoensombutamon, H. Emura, R. N. Alexander, S. Takeda, J.-i. Yoshikawa, N. C. Menicucci, H. Yonezawa, and A. Furusawa, Science **366**, 373 (2019).
[13] M. V. Larsen, X. Guo, C. R. Breum, J. S. Neergaard-Nielsen, and U. L. Andersen, Science **366**, 369 (2019).
[14] D. Gottesman, A. Kitaev, and J. Preskill, Phys. Rev. A **64**, 012310 (2001).
[15] K. Noh, S. M. Girvin, and L. Jiang, Phys. Rev. Lett. **125**, 080503 (2020).
[16] F. Guo, F. Mueller, and Y. Liu, Phys. Rev. Research **8**, 023158 (2026).
[17] S. L. Braunstein and P. van Loock, Rev. Mod. Phys. **77**, 513 (2005).
[18] C. Weedbrook, S. Pirandola, R. García-Patrón, N. J. Cerf, T. C. Ralph, J. H. Shapiro, and S. Lloyd, Rev. Mod. Phys. **84**, 621 (2012).
[19] Y. Liu, S. Singh, K. C. Smith, E. Crane, J. M. Martyn, A. Eickbusch, A. Schuckert, R. D. Li, J. Sinanan-Singh, M. B. Soley, T. Tsunoda, I. L. Chuang, N. Wiebe, and S. M. Girvin, PRX Quantum **7**, 010201 (2026).
[20] L. Chakhmakhchyan and N. J. Cerf, Phys. Rev. A **98**, 062314 (2018).
[21] Y. Y. Gao, B. J. Lester, Y. Zhang, C. Wang, S. Rosenblum, L. Frunzio, L. Jiang, S. M. Girvin, and R. J. Schoelkopf, Phys. Rev. X **8**, 021073 (2018).
[22] B. J. Chapman, S. J. de Graaf, S. H. Xue, Y. Zhang, J. Teoh, J. C. Curtis, T. Tsunoda, A. Eickbusch, A. P. Read, A. Koottandavida, S. O. Mundhada, L. Frunzio, M. H. Devoret, S. M. Girvin, and R. J. Schoelkopf, PRX Quantum **4**, 020355 (2023).
[23] Y. Yin, Y. Chen, D. Sank, P. J. J. O'Malley, T. C. White, R. Barends, J. Kelly, E. Lucero, M. Mariantoni, A. Megrant, C. Neill, A. Vainsencher, J. Wenner, A. N. Korotkov, A. N. Cleland, and J. M. Martinis, Phys. Rev. Lett. **110**, 107001 (2013).
[24] M. Pierre, I.-M. Svensson, S. R. Sathyamoorthy, G. Johansson, and P. Delsing, Appl. Phys. Lett. **104**, 232604 (2014).
[25] A. A. Houck, D. I. Schuster, J. M. Gambetta, J. A. Schreier, B. R. Johnson, J. M. Chow, L. Frunzio, J. Majer, M. H. Devoret, S. M. Girvin, and R. J. Schoelkopf, Nature **449**, 328 (2007).
[26] M. Pechal, L. Huthmacher, C. Eichler, S. Zeytinoğlu, J. Abdumalikov, A. A., S. Berger, A. Wallraff, and S. Filipp, Phys. Rev. X **4**, 041010 (2014).
[27] C. Schön, E. Solano, F. Verstraete, J. I. Cirac, and M. M. Wolf, Phys. Rev. Lett. **95**, 110503 (2005).

[28] C. Schön, K. Hammerer, M. M. Wolf, J. I. Cirac, and E. Solano, Phys. Rev. A **75**, 032311 (2007).

[29] G. Adesso and M. Ericsson, Phys. Rev. A **74**, 030305 (2006).

[30] N. H. Lindner and T. Rudolph, Phys. Rev. Lett. **103**, 113602 (2009).

[31] B. Li, S. E. Economou, and E. Barnes, npj Quantum Inf. **8**, 11 (2022).

[32] S. L. Braunstein, Phys. Rev. Lett. **80**, 4084 (1998).

[33] S. Lloyd and J.-J. E. Slotine, Phys. Rev. Lett. **80**, 4088 (1998).

[34] H. Pichler, S. Choi, P. Zoller, and M. D. Lukin, Proc. Natl. Acad. Sci. U.S.A. **114**, 11362 (2017).

[35] R. W. Heeres, P. Reinhold, N. Ofek, L. Frunzio, L. Jiang, M. H. Devoret, and R. J. Schoelkopf, Nat. Commun. **8**, 94 (2017).

[36] J. Eisert, M. Cramer, and M. B. Plenio, Rev. Mod. Phys. **82**, 277 (2010).

[37] A. Botero and B. Reznik, Phys. Rev. A **67**, 052311 (2003).

[38] J. Wu, A. J. Brady, and Q. Zhuang, Quantum **7**, 1082 (2023).

[39] A. J. Brady, J. Wu, and Q. Zhuang, Quantum **8**, 1478 (2024).

[40] P. W. Shor, Phys. Rev. A **52**, R2493 (1995).

[41] R. Bellman, J. Assoc. Comput. Mach. **9**, 61 (1962).

[42] M. Held and R. M. Karp, J. Soc. Indust. Appl. Math. **10**, 196 (1962).

[43] G. J. Chaitin, ACM SIGPLAN Not. **17(6)**, 98 (1982).

[44] J. Zhang and S. L. Braunstein, Phys. Rev. A **73**, 032318 (2006).

[45] N. C. Menicucci, S. T. Flammia, H. Zaidi, and O. Pfister, Phys. Rev. A **76**, 010302(R) (2007).

[46] M. Reck, A. Zeilinger, H. J. Bernstein, and P. Bertani, Phys. Rev. Lett. **73**, 58 (1994).

[47] W. R. Clements, P. C. Humphreys, B. J. Metcalf, W. S. Kolthammer, and I. A. Walmsley, Optica **3**, 1460 (2016).

[48] D. Maslov, G. W. Dueck, D. M. Miller, and C. Negrevergne, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **27**, 436 (2008).

[49] Y. Nam, N. J. Ross, Y. Su, A. M. Childs, and D. Maslov, npj Quantum Inf. **4**, 23 (2018).